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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,090	11/04/2003	Girolamo Gallo	400.196US01	4430
27073	7590	09/26/2005	EXAMINER	
LEFFERT JAY & POLGLAZE, P.A. P.O. BOX 581009 MINNEAPOLIS, MN 55458-1009			LE, DON P	
			ART UNIT	PAPER NUMBER
			2819	

DATE MAILED: 09/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/701,090

Applicant(s)

GALLO ET AL.

Examiner

Don P. Le

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 4-7, 9, 11, 13-15, 17-22, 25-29, 32-34, 39, 40, 42-44 and 46-48 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4-7, 17-22, 25-29, 32-34, 39, 40, 42-44 is/are allowed.
- 6) ☒ Claim(s) 9, 13, 14 and 46-48 is/are rejected.
- 7) ☒ Claim(s) 11 and 15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 9, 13, 14, 46 and 47 are rejected under 35 U.S.C. 102(b) as being anticipate by Michelsen (US 5,387,824).

3. With respect to claim 9, figure 2 of Michelsen discloses an output buffer, comprising:

at least two parallel buffer stages (26-27, 36-37), each stage activated upon receipt of a respective stage enable signal, the stages providing a range of output buffer strengths cumulatively to a total output buffer strength, wherein each output stage comprises:

a pair of CMOS components (26, 27), the first CMOS component connected to a hard coded buffer strength signal, and the second CMOS component connected to a selectable buffer strength signal; and

selection circuitry (21, 22) to select either the first CMOS component or the second CMOS component.

4. With respect to claim 13, figure 2 of Michelsen discloses an output buffer circuit, comprising:

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a first output buffer stage (26, 27) for providing an output buffer strength in response to a first stage enable signal (EN1); and

at least one second output buffer stage (36, 37), wherein each second output buffer stage is adapted to selectively provide additional buffer strength in response to a respective second stage enable signal (EN2), wherein each output stage comprises:

a pair of CMOS components, the first CMOS component (26) connected to a hard coded buffer strength signal, and the second CMOS component (27) connected to a selectable buffer strength signal; and

selection circuitry (21, 22) to select either the first CMOS component or the second CMOS component.

5. With respect to claim 14, figure 2 of Michelsen discloses an output buffer circuit, comprising:

a plurality of output stages (26-27, 36-37), each output stage selectable to provide a component of a total output buffer strength, each output stage comprising:

a pair of CMOS components, the first CMOS component connected to a hard coded buffer strength enable signal, and the second CMOS component connected to a selectable buffer strength enable signal; and

selection circuitry (21, 22) to select either the first CMOS component or the second CMOS component.

6. With respect to claims 46-48, the methods therein are inherent given the apparatus of Michelsen as shown in the above rejections.

Allowable Subject Matter

7. Claims 4-7, 17-22, 25-29, 32-34 and 39-44 are allowed.
8. Claims 11 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
9. The following is an examiner's statement of reasons for allowance:

With respect to claims 4, 7, 11, 15, 17, 21, 25, 28, 32 and 40, the prior art does not teach a bank of latches.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

10. Applicant's arguments filed 8/5/2005 have been fully considered but they are not persuasive.

With respect to claims 9 and 14, applicant argues that the prior art does not teach "hard coded buffer strength signal and a selectable buffer strength signal." **In reading of the claim language, the claim does not specifically describe as to what exactly is a "hard coded buffer strength signal and a selectable buffer strength signal."** These are just arbitrary names for the two signals. The prior art discloses a buffer circuit comprising two CMOS and control by two signals (same as applicant). Broad interpretations of the claim language would read on the prior art because the prior art does use two signals to control the CMOS.

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With respect to claims 46 and 47, applicant argues that the prior art does not teach “selecting predetermined or programmable enable inputs...” Again these are just arbitrary names for signals with no specific description in the claims as to what these signals behave or come from. Therefore, the same argument applied to these claims as claims 9 and 14 above. All the prior art signals have predetermined values.

Applicant did not provide reasons why claim 13 is allowable.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

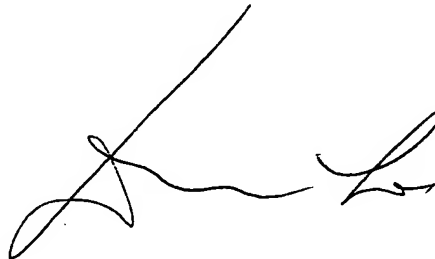
12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

9/23/3005

A handwritten signature in black ink, appearing to read 'DON LE', with a stylized flourish at the end.

DON LE
PRIMARY EXAMINER